REMARKS

Claims 1-26 are pending. Claims 1 and 3-8 have been amended. Claims 9-20 have been withdrawn from further consideration. Claims 21-26 are newly presented. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Election Requirement

Applicants acknowledge that in a conversation on June 18, 2002 with the Examiner, Applicants' Representative elected claims 1-8 without traverse.

In The Specification

The title of the application was objected to for allegedly being non descriptive. Applicants have amended the title so as to be more descriptive. Additionally, Applicants have amended the specification for clarity and to correct minor informalities. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims Rejections Under 35 U.S.C. § 112

Claims 1-8 were rejected under 35 U.S.C. § 112, second paragraph. Specifically, The Examiner alleges that the phrases "width-increased groove portion" in claims 1 and 3-5, "island-like" in claims 6-8, "continuously disposed along one direction and also with a bit line coupled to the second diffusion layer of said transistor being provided to cross said word line" in claim 6, and "bit line is in contact with said diffusion layer per each DRAM cell" in claim 7 are unclear. Claims 1 and 6-8 have been amended for clarity to more clearly recite the intended features of these claims. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claim Rejections Under 35 U.S.C. § 103

A. Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) over Lee (U.S. Patent No. 5,959,322) in view of Womack et al. (U.S. Patent No. 4,713,678). Applicants respectfully traverse this rejection.

Claim 1 recites, in part, a semiconductor device which includes an element substrate with a semiconductor layer, a semiconductor substrate, and a dielectric formed between them. Further, the element substrate has a groove formed therein, which extends from a top surface

of the semiconductor layer into the dielectric film and the grove has a portion within the dielectric film with an increased width, so as expose a bottom surface of the semiconductor layer. The portion of the groove with an increased width has an impurity diffusion source buried within it and the impurity diffusion source is in contact with the bottom surface of the semiconductor layer. The Examiner alleges that Lee discloses a groove with an increased width portion in the dielectric film. Applicants respectfully disagree.

Lee shows a trench T (Figure 14, column 7, lines 34-45) which is filled with an insulating material. The trench has a wider portion but the portion is located within the conductive layer 56 (Figure 16). Accordingly, the trench disclosed in Lee is not the same as the groove of claim 1 since (1) it does not have a portion with an increased with located within the dielectric film and (2) it is filled with an insulating material not a impurity diffusion source, as recited in claim 1. Additionally, Womack, does not disclose a groove with a portion having an increased width, as recited in claim 1. Accordingly, no combination of Lee and Womack teach or suggest, at least, a groove which extends from a top surface of the semiconductor layer into the dielectric film and the grove has a portion within the dielectric film with an increased width, so as expose a bottom surface of the semiconductor layer, as recited in claim 1.

Claim 2 is believed allowable for at least the same reasons presented above with respect to claim 1 by virtue of its dependence upon claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection

B. Claim 3 was rejected under 35 U.S.C. § 103(a) over Lee in view of Womack and further in view of Applicants admitted Prior Art and claims 6-8 were rejected under 35 U.S.C. § 103(a) over Lee in view of Womack and Hieda et al. (U.S. Patent No. 5,508,541). Applicants respectfully traverse these rejections.

Claims 3 and 6-8 are believed allowable for at least the same reasons presented above with respect to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Applicants appreciate the Examiner's indication that claims 4 and 5 contain allowable subject matter and would be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claim. However, in view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited.

If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

Pillsbury Winthrop LLP

By: _____

Dale S. Lazar
Reg. No.: 28,872
Tel. No.: (703) 905-2126
Fax No.: (703) 905-2500

DSL\VVK
1600 Tysons Boulevard
McLean, VA 22102

(703) 905-2000
Enclosure: Appendix

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The Title has been amended as follows:

SEMICONDUCTOR DEVICE [AND METHOD OF FABRICATING THE SAME] WITH VERTICAL TRANSISTOR FORMED IN A SILICON-ON-INSULATOR SUBSTRATE

IN THE SPECIFICATION:

The paragraph beginning on page 1, line 9 has been amended as follows:

This invention relates in general to semiconductor microtechnologies and, [in more particular] more specifically, to highly integrated semiconductor devices with dynamic random access memory (DRAM) cells each having a trench capacitor and a vertical transistor that works perpendicular to the surface of a semiconductor chip. The invention also relates to methodology for fabrication of semiconductor devices of the type stated above.

The paragraph beginning on page 1, line 18 has been amended as follows:

In recent years, DRAM devices employing memory cells each consisting essentially of a single transistor and a single capacitor, also known as "1-transistor/1-capacitor" cells, are becoming [greater] denser in integration or "bit-packing" density virtually endlessly. On-chip areas of such memory cells are made smaller once per development of a new generation of products. One basic approach to reducing cell areas is to lower the occupation areas of transistors and capacitors, which make up the cells, respectively.

The paragraph beginning on page 3, line 16 has been amended as follows:

High-density DRAM cell structures capable of avoiding these problems have been proposed until today, one of which is disclosed in U. Gruening et al., "A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb," IEDM Tech. Dig., 1999. This trench DRAM cell is arranged so that a capacitor is formed at a lower part of a trench defined in a substrate while forming, at an upper part of the trench, a vertically structured transistor with a trench side face as its channel.

The paragraph beginning on page 5, line 23 and ending on page 6, line 17 has been amended as follows:

A semiconductor device in accordance with one aspect of the present invention has: an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween; said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove being formed to have [a width-increased groove] an increased width portion in said dielectric film as to expose a bottom surface of said semiconductor layer; an impurity diffusion source buried in said [width-increased groove] increased width portion of said groove to be contacted with said bottom surface of said semiconductor layer; and a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

The paragraph beginning on page 6, line 18 and ending on page 7, line 9 has been amended as follows:

A method of fabricating a semiconductor device in accordance with another aspect of the present invention including: forming a groove in an element substrate having a semiconductor layer of a first conductivity type as insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, the groove being penetrating the semiconductor layer; selectively etching the dielectric film exposed at the groove to form [a width-increased groove] an increased width portion for permitting exposure of a bottom surface of the semiconductor layer; forming an impurity diffusion source buried in the [width-increased groove] increased width portion of the groove while letting the impurity diffusion source be in contact with only the bottom surface of the semiconductor layer; forming and burying in the groove a gate electrode along with an underlying gate insulation film; and forming in said semiconductor layer source and drain diffusion layers through impurity diffusion to a top surface and also impurity diffusion to the bottom surface by use of said impurity diffusion source.

The paragraph beginning on page 9, line 8 has been amended as follows:

Several embodiments of this invention will now be set forth with reference to the accompanying figures [of the drawing below].

The paragraph beginning on page 9, line 12 has been amended as follows:

Referring now to Fig. 1, there is shown a plan view of a main part of a trench-capacitor-based dynamic random access memory (DRAM) cell array with half-pitch folded bit line structure in accordance with one embodiment of this invention. Also see Figs. 2 and 3, which depict cross-sectional views of the structure of Fig. 1 as taken along lines I-I' and II-II' respectively.

IN THE CLAIMS:

Claims 1 and 3-8 have been amended as follows:

1. (Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove being formed to have [a width-increased groove] an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer;

an impurity diffusion source buried in said [width-increased groove] increased width portion of said groove to be contacted with said bottom surface of said semiconductor layer; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

3. (Amended) The semiconductor device according to claim 2, wherein a buried strap for use as said impurity diffusion source is formed and buried in said [width-increased groove] increased width portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film with the gate electrode of said transistor embedded to overlie said cap insulation film.

4. (Amended) The semiconductor device according to claim 3, wherein said buried strap comprises a first strap buried on said storage electrode and a second strap stacked on the first strap and buried in said [width-increased groove] increased width portion being in contact with said semiconductor layer only at the bottom surface thereof.

5. The semiconductor device according to claim 3, wherein said [width-increased groove] increased width portion of said groove is formed to cover an entire range of a thickness of said dielectric film whereas the storage electrode of said capacitor is half buried in said [width-increased groove] increased width portion with said buried strap being embedded on said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof.

6. (Amended) The semiconductor device according to claim 2, wherein said semiconductor layer is partitioned into a plurality of [island-like] element regions by an element isolating insulative film [as] formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said [island-like] element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor [being continuously disposed along one direction and also with a bit line] and a bit line coupled to the second diffusion layer of said transistor [being provided to cross said word line] said word line and said bit line being continuously disposed to cross each other.

7. (Amended) The semiconductor device according to claim 6, wherein said bit line is in contact with said second diffusion layer [per] of each DRAM cell at a position adjacent to word lines at both ends of each said [island-like] element region, and wherein a body wire lead is formed to be contacted with said semiconductor layer across central part of said [island-like] element region for applying a fixed potential to said semiconductor layer.

8. (Amended) The semiconductor device according to claim 2, wherein said semiconductor layer is partitioned into a plurality of [island-like] element regions by an element isolating insulative film [as] formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said [island-like] element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor [being continuously disposed along one direction and also with] and a bit line coupled to the second diffusion layer of said transistor [being provided to cross said word line] said word line and said bit line being continuously disposed to cross each other.

Claims 21-26 are newly presented.

End of Appendix